# DESCRIPTION

The BDR6622T is a dual bridge motor driver which has two H-bridge drivers, and can drive two DC brush motors, a bipolar stepper motor, solenoids, or other inductive loads.

It operates from 2.7V to 15V, and can deliver load current up to 700mA per channel. The output driver block of each H-bridge consists of N-channel power MOSFETS configured as an H-bridge to drive the motor windings. Each H-bridge includes circuitry to regulate or limit the winding current.

The internal safety features include sinking and sourcing current limits implemented with external sensors, under-voltage lockout, over current protection (OCP) and thermal shutdown. An over-temperature output flag is available to indicate thermal shutdown.

The BDR6622T is packaged in 16-pin, 5.0mm×6.4mm TSSOP-EP and TSSOP, 3mm×3mm and 4mmx4mm QFN package with an exposed thermal pad on the back.

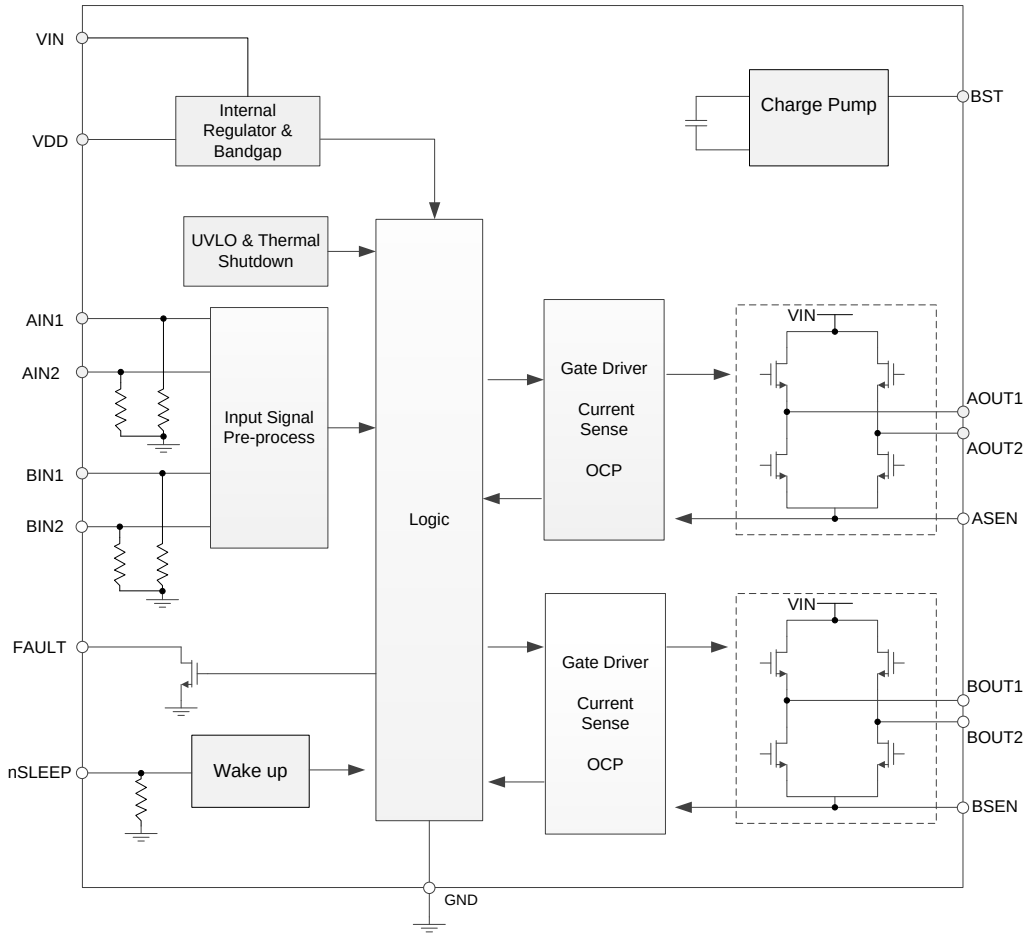
# FEATURES

- Wide Power Supply Voltage Range: 2.7V to 15V
- Two Internal Full-Bridge Drivers
- Internal Charge Pump for the High-Side Driver
- Low Quiescent Current: 1.1mA
- Low Sleep Current: 1μA
- Thermal Shutdown and Under-Voltage Lockout Protection
- Over Current Protection (OCP)
- Over-Temperature Output Flag
- Thermally-Enhanced Surface-Mount Package
- Low MOSFET On Resistance (HS: 600mΩ;LS: 570 mΩ)

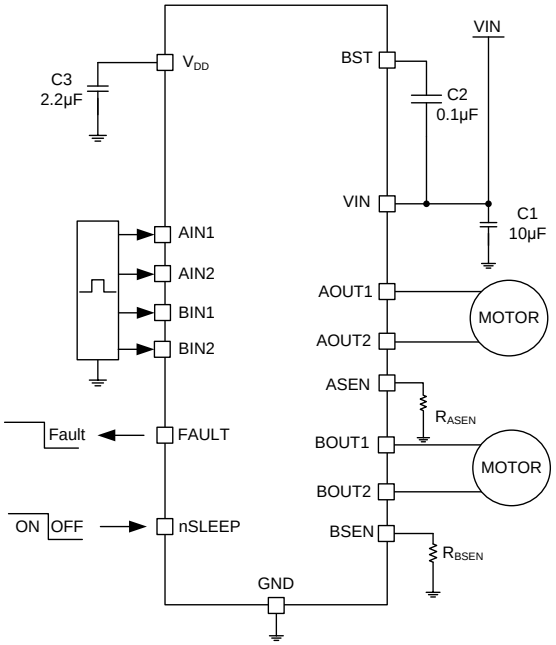
# APPLICATIONS

- Digital Still Cameras
- POS Printers
- Video Security Camera
- Robotics
- Battery Powered Toys

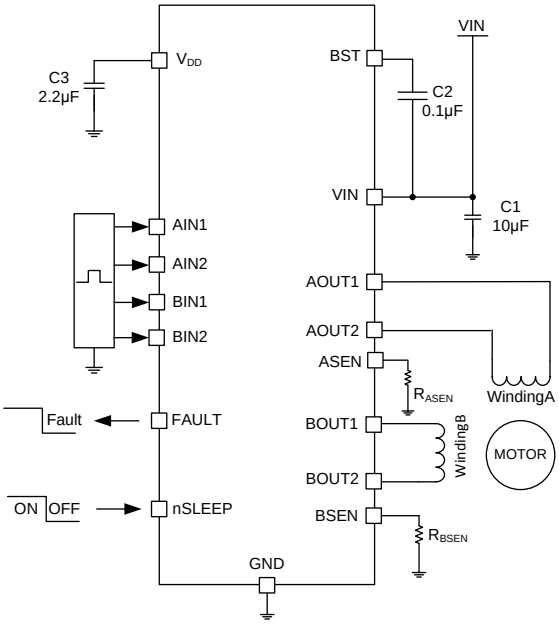
# BLOCK DIAGRAM



# APPLICATION CIRCUIT




**Dual DC Motor Application**

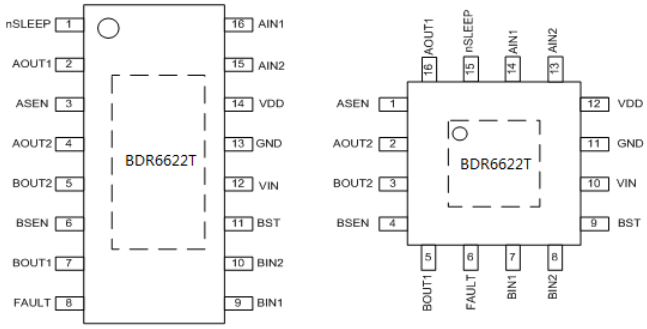



**Stepper Motor Application**

# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| BDR6622T-HT | 16-Pin, HTSSOP | BDR6622T-HT |
| BDR6622T-TX | 16-Pin, TSSOP | BDR6622T-TX |
| BDR6622T | 16-Pin, QFN (3x3mm) | BDR6622T |
| BDR6622T | 16-Pin, QFN(4x4mm) | BDR6622T |

# PIN CONFIGURATION




Note: The exposed pad for TSSOP16-EP and QFN package need to be connected to GND.

# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. | |
|---|---|---|---|---|
| | | | QFN-16 | TSSOP-16 |
| ASEN | I/O | Channel A current sense. Connect to current sensor resistor for Channel A | 1 | 3 |
| AOUT2 | O | Connecting to motor winding A. | 2 | 4 |
| BOUT2 | O | Connecting to motor winding B. | 3 | 5 |
| BSEN | I/O | Channel B current sense. Connect to current sensor resistor for Channel B | 4 | 6 |
| BOUT1 | O | Connecting to motor winding B. | 5 | 7 |
| FAULT | OD | Fault output. Logic low when in over-temperature fault condition. | 6 | 8 |
| BIN1 | I | Bridge B input 1 to control BOUT1. (200K internal pull down resistor to GND.) | 7 | 9 |
| BIN2 | I | Bridge B input 2 to control BOUT2. (200K internal pull down resistor to GND.) | 8 | 10 |
| BST | I/O | Charge Pump Output. Connect a 10nF to 100nF ceramic capacitor to VIN. | 9 | 11 |
| VIN | Power | Device power supply. Ranges from 2.7V to 15V. A 10-µF ceramic bypass capacitor to GND is recommended. | 10 | 12 |
| GND | GND | Device ground. (Both the GND pin and device Power PAD must be connected to ground.) | 11 | 13 |
| VDD | Power | Internal control and logic supply voltage. Connect a 2.2µF capacitor from VDD to GND. VDD is for internal use only. Do not connect any external load to VDD pin. | 12 | 14 |
| AIN2 | I | Bridge A input 2 to control AOUT2. (200K internal pull down resistor to GND.) | 13 | 15 |
| AIN1 | I | Bridge A input 1 to control AOUT1. (200K internal pull down resistor to GND.) | 14 | 16 |
| nSLEEP | I | Sleep mode input. Logic high to enable device, logic low to enter low-power sleep mode and reset all internal logic.(200K internal pull down resistor to GND.) | 15 | 1 |
| AOUT1 | O | Connect to motor winding A. | 16 | 2 |

# OPERATION DESCRIPTION

The BDR6622T device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two NMOS H-bridges and current regulation circuitry. The BDR6622T can be powered with a supply voltage from 2.7 to 15 V and can provide an output current up to 700mA.

The motor output current can be either controlled by an external pulse width modulator (PWM) or internal PWM current controller. The current regulation (internal PWM current control) is a fixed off time PWM slow decay.

The BDR6622T includes a lower power sleep mode, which lets the system save power when not driving the motor. It also provides the fault protections include: under-voltage lockout (UVLO) and over-temperature protection (OTP).

## *EXTERNAL PWM CURRENT CONTROL*

The motor current can be regulated by applying external PWM signals on the input pins AIN1, AIN2, BIN1 and BIN2. The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2. Table 1 shows the logic.

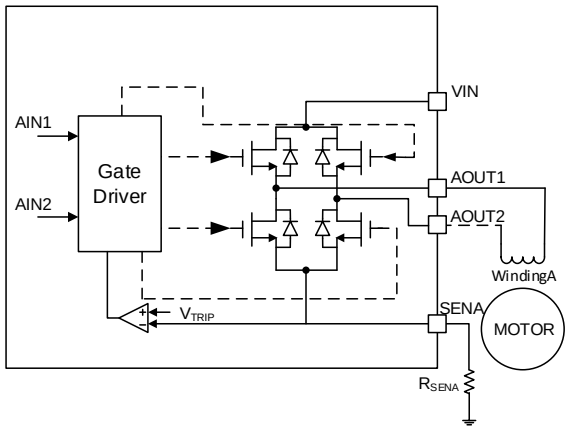



**Figure1: Full-Bridge Control Circuit**

| A/BIN1 | A/BIN2 | A/BOUT1 | A/BOUT2 |
|---|---|---|---|
| L | L | High Impedance | High Impedance |
| L | H | GND | VIN |
| H | L | VIN | GND |
| H | H | GND | GND |

**Table1: Full-Bridge Gate Logic**

In external PWM control mode, the winding's inductive current ramps up when the high-side MOSFET is on and freewheels during the high side MOSFET's off time to cause the recirculation current.

To handle this recirculation current, the H-bridge can operate in two different states: fast decay and slow decay, both of which are shown in Figure 2 for forward operation and Figure 3 for reverse operation.

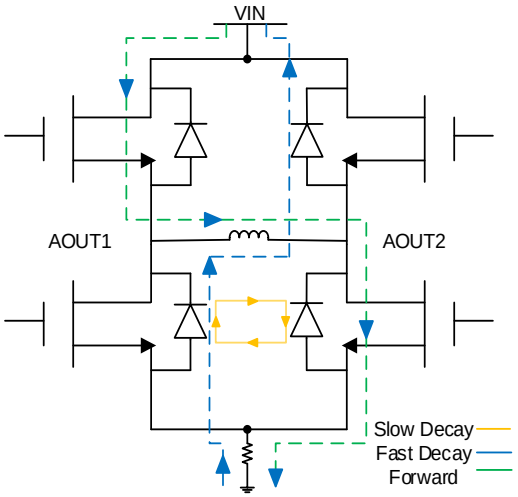



**Figure2: Forward Operation**

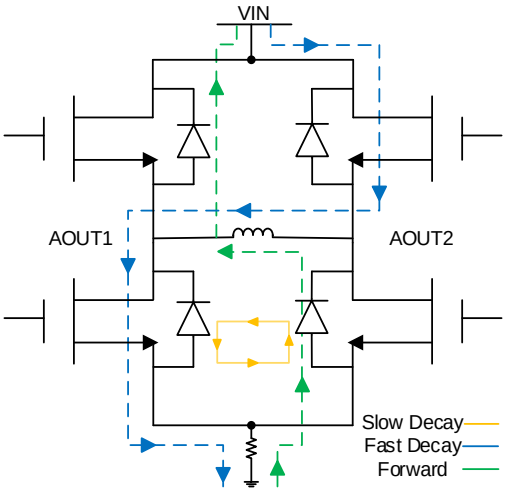



**Figure3: Reverse Operation**

For fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes. For slow decay mode, the current circulates through the two low-side MOSFETS. To PWM using fast decay, the PWM signal is applied to one input pin while the other is held low. To using slow decay mode, one input is held high and apply the PWM signal to other input pin. See Table 2 for more configuration details and Figure 4 for detailed wave forms.

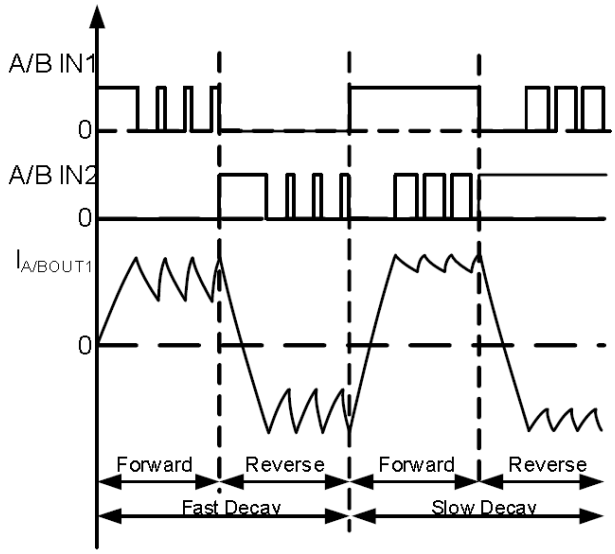



**Figure 4: External PWM Current Control Waveform**

| A/BIN1 | A/BIN2 | Mode |
|---|---|---|
| H (PWM) | L | Forward |
| L (PWM) | L | Fast Decay |
| L | H (PWM) | Reverse |
| L | L (PWM) | Fast Decay |
| H | L (PWM) | Forward |
| H | H (PWM) | Slow Decay |
| L (PWM) | H | Reverse |
| H (PWM) | H | Slow Decay |

**Table 2: PWM Control**

## *INTERNAL PWM CURRENT CONTROL*

An internal constant off-time PWM current control circuit will regulate the motor current as the following:
When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. The current increases in the motor winding, which is sensed by an external sense resistor (RSENSE). During the initial blanking time TBLANK (2.7μs), the high-side MOSFET always turns on in spite of current limit detection. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.

After the blanking time, if the voltage across RSENSE reaches the internal reference voltage threshold VTRIP (185mV), the bridge disables the current by shuts off the high-side MOSFET. After that, the H-bridge switches to slow decay mode. Winding current is decreases and recirculated by enabling both of the low-side FETs in the bridge. In this slow decay mode, the current freewheels through one low-side MOSFET and the body diode of the other low-side MOSFET to short the winding. This mode enables both two low-side MOSFETs, which feature a lower voltage drop and lower power dissipation during decay operation.

The slow decay mode is held until the internal clock reaches it's constant off time (typically 21μs). After the fixed off time the high-side MOSFET is enable and the winding current will increase again. The cycle then repeats.

Calculate the current limit as: $\mathrm{I_{LIMIT}} = \frac{\mathrm{Vtrip}}{\mathrm{Rsense}}$

Example: If a 1-Ω sense resistor is used, the chopping current will be 185 mV/1 Ω = 185 mA.
If current control is not needed, the xSEN pins should be connected directly to ground.

## SLEEP MODE

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until n SLEEP returns inactive high. When returning from sleep mode, some time (up to 1 ms) needs to pass before the motor driver becomes fully operational.

## BLANKING TIME

An internal blanking time $T_{BLANK}$ blanks the output of the current sense comparator when the outputs are switched, which is also the minimum on time for high-side MOSFET. There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This blanking time is filtering the current spike and prevents it from erroneously shutting down the high-side MOSFET.

## OVER CURRENT PROTECTION (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time (2.7μs), all FETs in the H-bridge will be disabled and the FAULT pin will be driven low. The driver will be re-enabled after the OCP retry period ($t_{OCP}$) has passed. FAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and FAULT remains de-asserted. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

Over current conditions are detected independently on both high- and low-side devices; that is, a short to ground, supply, or across the motor winding will all result in an over current shutdown. Over current protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xSEN resistors.

## THERMAL SHUTDOWN (TSD)

If the die temperature exceeds safe limits(typically 170ºC), all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level (typically 140ºC), operation will automatically resume.

## UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VM pin falls below the under voltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT is driven low in the event of an under voltage condition.

# APPLICATION INFORMATION

**Driver Mode:**

The BDR6622T could be configured for both full step and half-step modes by sequentially energizing the two windings. Full-step drive energizes two winding phases at any given time. The stator windings are energized as per the sequence shown in Table 3. There are a total of four steps for one cycle in the sequence: $AB \rightarrow \overline{A}B \rightarrow \overline{AB} \rightarrow A\overline{B}$.

Half-step energizes the stator windings as per the sequence shown in Table 4. There are a total of 8 steps for one cycle: $AB \rightarrow B \rightarrow \overline{A}B \rightarrow \overline{A} \rightarrow \overline{AB} \rightarrow \overline{B} \rightarrow A\overline{B} \rightarrow A$.

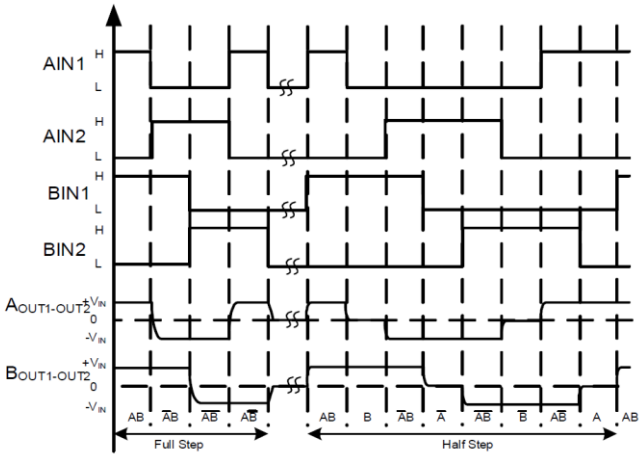



**Figure 5: Signal Logic Sequences for Full-Step and Half-Step**

| Sequence(Full Step) | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| A | ✓ | | | ✓ |
| B | ✓ | ✓ | | |
| $\overline{A}$ | | ✓ | ✓ | |
| $\overline{B}$ | | | ✓ | ✓ |

**Table 3: Full-Step Drive Sequence**

| Sequence(Half Step) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| A | ✓ | | | | | | ✓ | ✓ |
| B | ✓ | ✓ | ✓ | | | | | |
| $\overline{A}$ | | | ✓ | ✓ | ✓ | | | |
| $\overline{B}$ | | | | | ✓ | ✓ | ✓ | |

**Table 4: Half-Step Drive Sequence**

Note: ✓ item is the selected winding voltage.

# POWER SUPPLY AND LAYOUT GUIDE

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied. The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor. The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

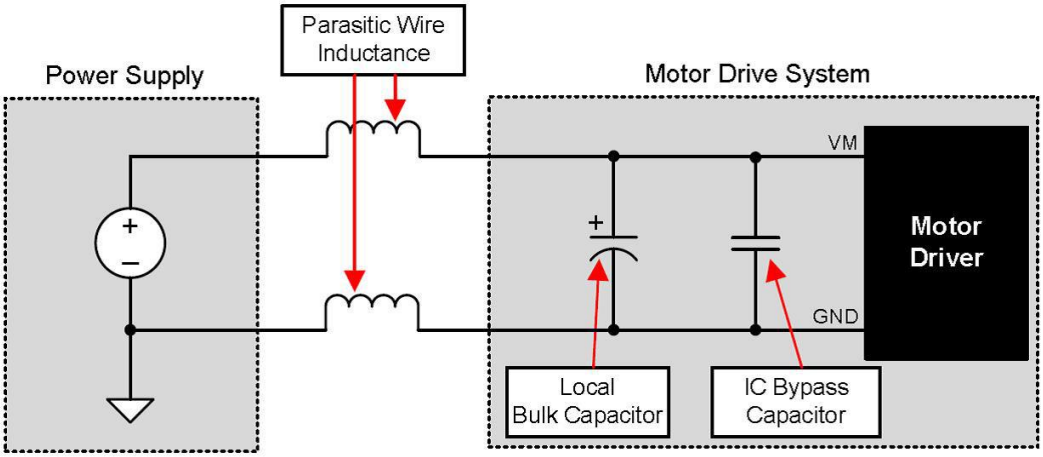



**Figure 6 : Example Setup of Motor Drive System with External Power Supply**

The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 10-μF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.
A low-ESR ceramic capacitor must be placed in between the VM and BST pins. PTC recommends a value of 0.1μF rated for 25 V. Place this component as close to the pins as possible.
Bypass VDD to ground with a 2.2-μF ceramic capacitor rated 6.3V. Place this bypass capacitor as close to the pin as possible.

The printed circuit board (PCB) should use a heavy ground-plane. The BDR6622T must be soldered directly onto the board for better electrical and thermal performance. The sense resistors should be placed as close as possible to the part for accurate current detection. The BDR6622T uses an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to copper on the PCB. Thermal vias are often used to transfer heat to other layers of the PCB.

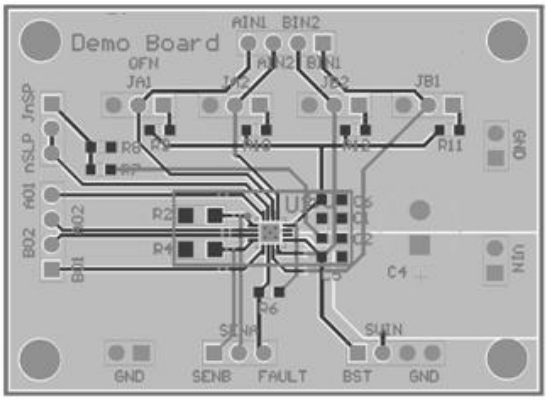



**Figure 7: QFN-16**

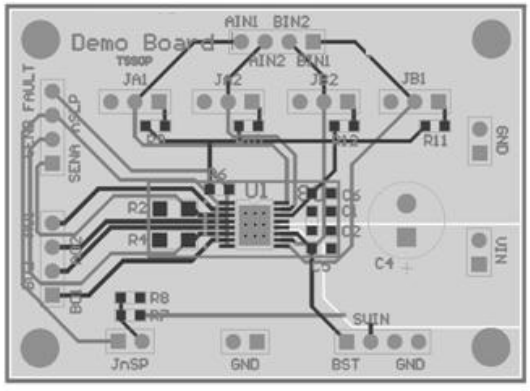



**Figure 8: TSSOP-16**

# *DESIGN EXAMPLE*

Below is a design example following the application guidelines for the specifications:
The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section.
$V_{IN}$ = 2.7V-15V, $I_{OUT}$= 400mA

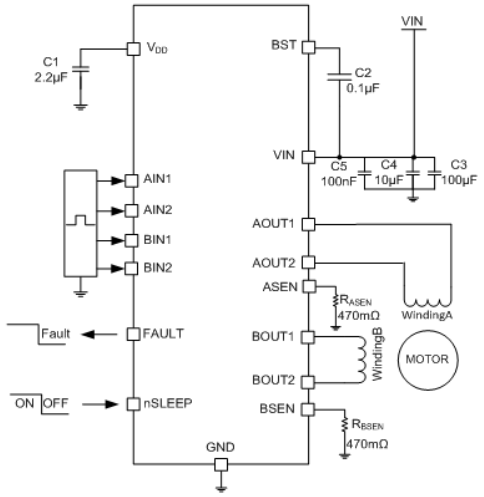



**Figure 9: Detailed Application Schematic**

# ABSOLUTE MAXIMUM RATING

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{IN}$ | -0.3 ~ +18 | V |
| AOUTx Voltage | $V_{AOUTx}$ | -0.3 ~ +$V_{IN}$+1V | V |
| BOUTx Voltage | $V_{BOUTx}$ | -0.3 ~ +$V_{IN}$+1V | V |
| BST Voltage | $V_{BST}$ | -0.3 ~ +$V_{IN}$+7V | V |
| Sense Voltage | $V_{SENx}$ | -0.3 ~ +0.5 | V |
| All Other Pins | - | -0.3 ~ +6.5 | V |
| Junction Temperature | $T_J$ | 150 | ℃ |
| Lead Temperature | $T_L$ | 260 | ℃ |
| Operating Temperature | $T_{OPR}$ | -40 ~ +85 | ℃ |
| Storage Temperature | $T_{STG}$ | -40 ~ +150 | ℃ |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

# RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Supply Voltage | $V_{IN}$ | 2.7 | - | 15 | V |
| Output Current | $I_{A/BOUT}$ | - | 700 | - | mA |
| Operating Junction Temperature | $T_J$ | -40 | 50 | 125 | ℃ |

# THERMALRESISTANCE

| Parameter | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| QFN 16(3X3mm) | 60 | 12 | ℃/W |
| QFN 16(4X4mm) | 46 | 10 | ℃/W |
| TSSOP 16-EP (5.0x6.4mm) | 45 | 10 | ℃/W |
| TSSOP 16 | 103 | 38 | ℃/W |

Note: Measure on JESD51-7, 4-layer PCB

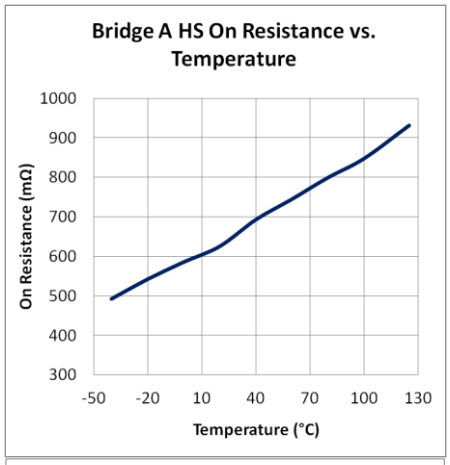
# ELECTRICAL CHARATERISTICS

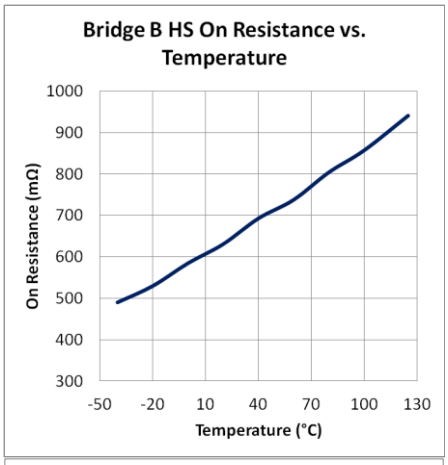
Nominal conditions: $V_{IN}$=5V, Ta=+25℃

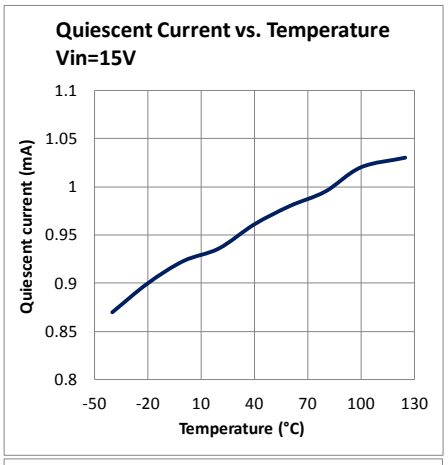
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input Supply Voltage | $V_{IN}$ | - | 2.7 | - | 15 | V |
| Quiescent Current | $I_{IN}$ | nSLEEP=1, $I_{OUT}$=0, Output disable | - | - | 1.1 | mA |
| | $I_{IN\_SLEEP}$ | nSLEEP=0, VIN=5V | - | - | 1 | μA |
| **Integrated MOSFETs** | | | | | | |
| Body-Diode Forward Voltage | $V_F$ | $I_{OUT}$=500mA | - | - | 1 | V |
| Output On Resistance | $R_{HS}$ | $I_{OUT}$=500mA, $V_{IN}$=5V $T_J$=25°C | - | 600 | - | mΩ |
| | | $I_{OUT}$=500mA, $V_{IN}$=5V $T_J$=85°C | - | 780 | - | mΩ |
| | $R_{LS}$ | $I_{OUT}$=500mA, $V_{IN}$=5V $T_J$=25°C | - | 570 | - | mΩ |
| | | $I_{OUT}$=500mA, $V_{IN}$=5V $T_J$=85°C | - | 730 | - | mΩ |
| **Control Logic** | | | | | | |
| UVLO Threshold (Rising) | $V_{IN\_RISE}$ | - | - | - | 2.7 | V |
| UVLO Hysteresis | $V_{HYS}$ | - | - | 80 | - | mV |
| Input Logic 'Low' Threshold | $V_{IL}$ | - | - | - | 0.6 | V |
| Input Logic 'High' Threshold | $V_{IH}$ | - | 2 | - | - | V |
| nSLEEP Logic, Low | $V_{SLEEP\_L}$ | - | - | - | 0.4 | V |
| nSLEEP Logic, High | $V_{SLEEP\_H}$ | - | 2 | - | - | V |
| Input pull down resistance | $R_{PD}$ | nSLEEP and Logic input pin | - | 200 | - | kΩ |
| Fault Output Logic, Low | $V_{FAULT\_L}$ | Flag triggered by OTP 1mA Current | - | - | 200 | mV |
| Fault Output Leakage Current | $I_{LEAK\_FAULT}$ | VFAULT=5V | - | - | 1 | μA |
| Constant Off Time | $T_{OFF}$ | - | - | 21 | - | μs |
| Propagation Delay Time (On) | $T_{ON\_DELAY}$ | INx high to OUTx on 10mA Source Current | - | 80 | - | ns |
| Propagation Delay Time (Off) | $T_{OFF\_DELAY}$ | INx low to OUTx off | - | 250 | - | ns |
| Cross Over Delay | $T_{CROSS}$ | HS off to LS on or LS off to HS on for one bridge arm | 200 | 300 | 650 | ns |
| Sleep Mode Wakeup Time | $T_{WAKE}$ | Sleep inactive high to full bridge turn on (VBST=100nF) | - | 1 | 1.5 | ms |

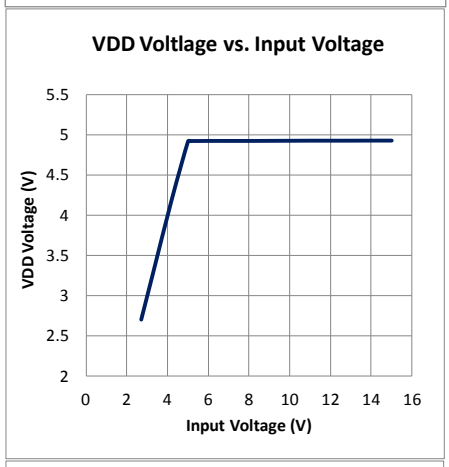
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Protection Circuitry** | | | | | | |
| Current Limit Sense Trip Voltage | $V_{TRIP}$ | - | - | 185 | - | mV |
| Blanking Time | $T_{BLANK}$ | - | 2.1 | 2.7 | 3.3 | μs |
| Over current protection trip level | $I_{OCP}$ | | - | 1.7 | - | A |
| Over current protection period | $T_{OCP}$ | - | - | 1.6 | - | ms |
| Thermal Shutdown | TSD | - | - | 170 | - | ℃ |
| Thermal Shutdown Hysteresis | - | - | - | 30 | - | ℃ |

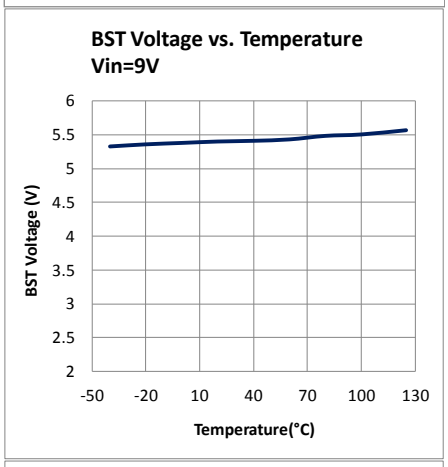
# TYPICAL CHARACTERISTICS

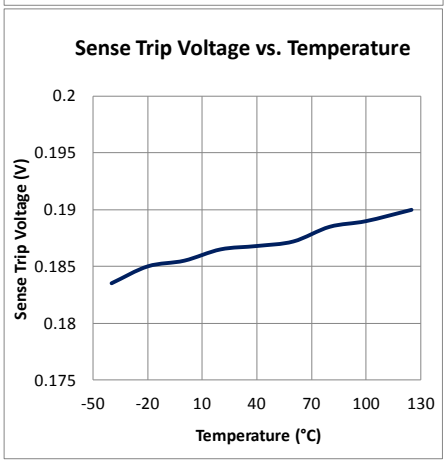


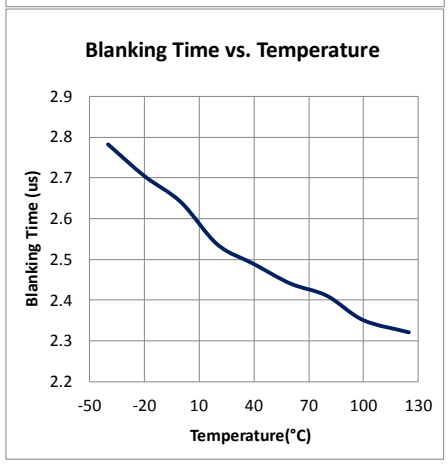



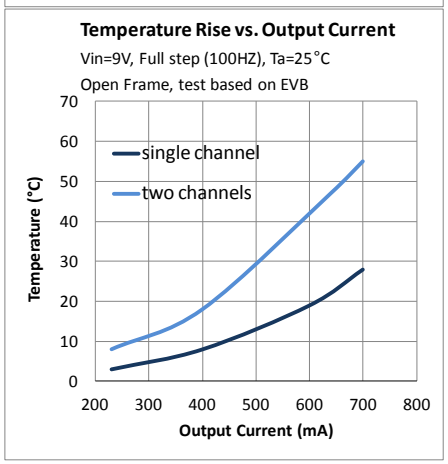



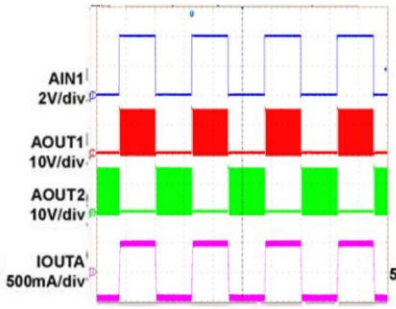



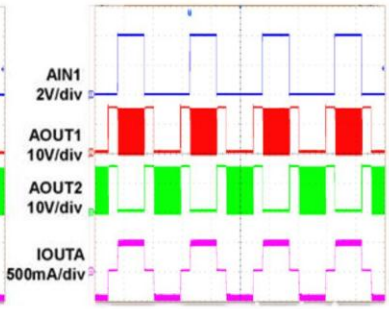
# TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
IOUT=500mA, FSTEP=100Hz, Stepper Motor: L=2mH, R=10Ω, TA=25°C, unless otherwise noted.

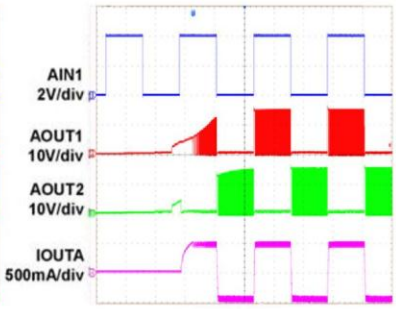
**Steady State-Full Step**
$V_{IN}$=15V



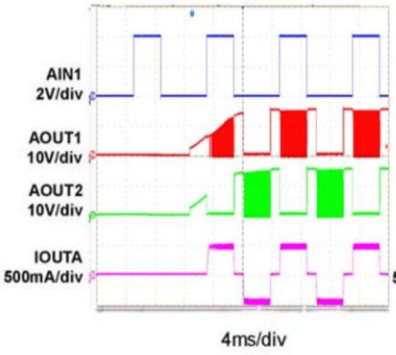

**Steady State-Half Step**
$V_{IN}$=15V



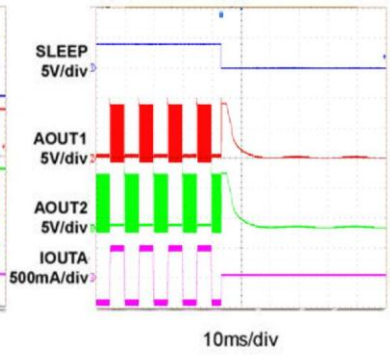

**Power Ramp Up-full Step**
$V_{IN}$=15V



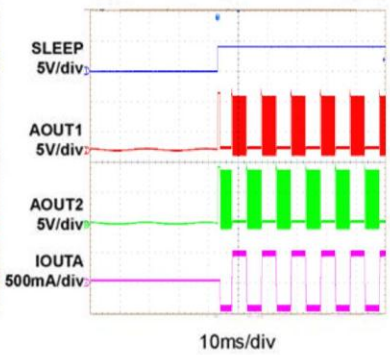

**Power Ramp Up-Half Step**
$V_{IN}$=15V



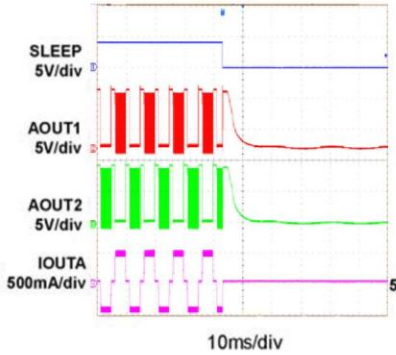

**Sleep Entry-Full Step**
$V_{IN}$=9V



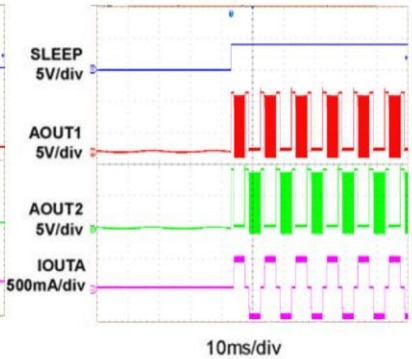

**Sleep Recovery-Full Step**
$V_{IN}$=9V




**Sleep Entry-Half Step**
$V_{IN}$=9V

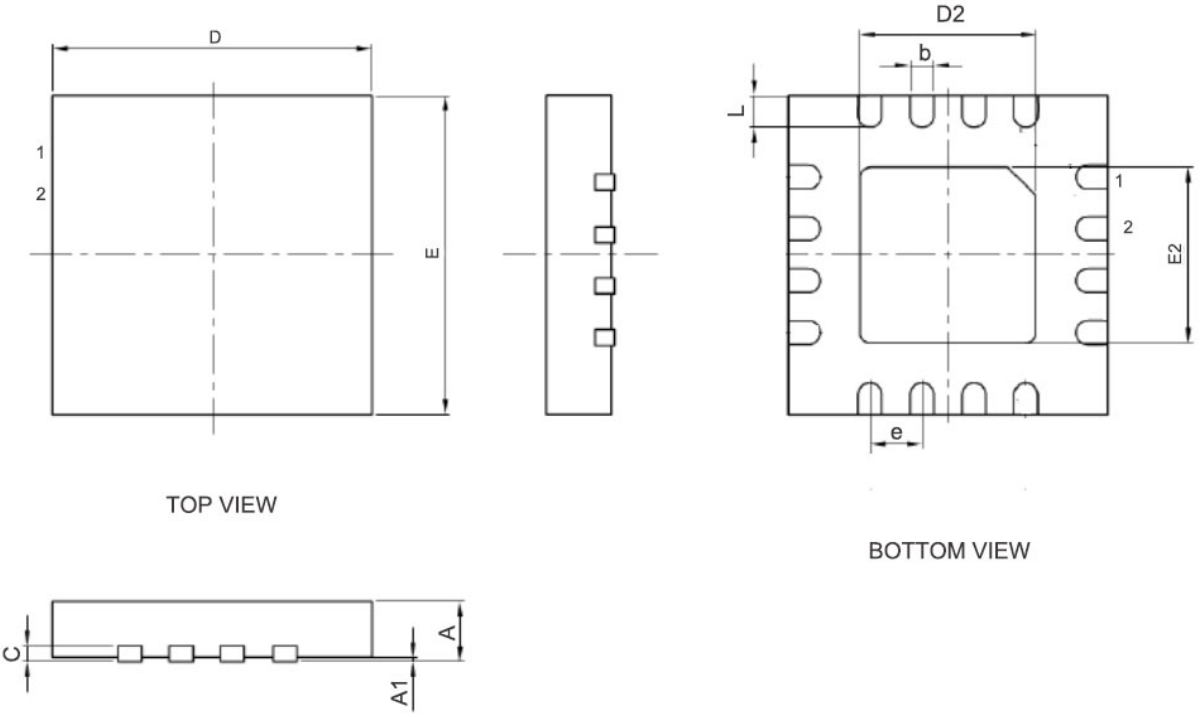



**Sleep Recovery-Half Step**
$V_{IN}$=9V



# PACKAGE INFORMATION

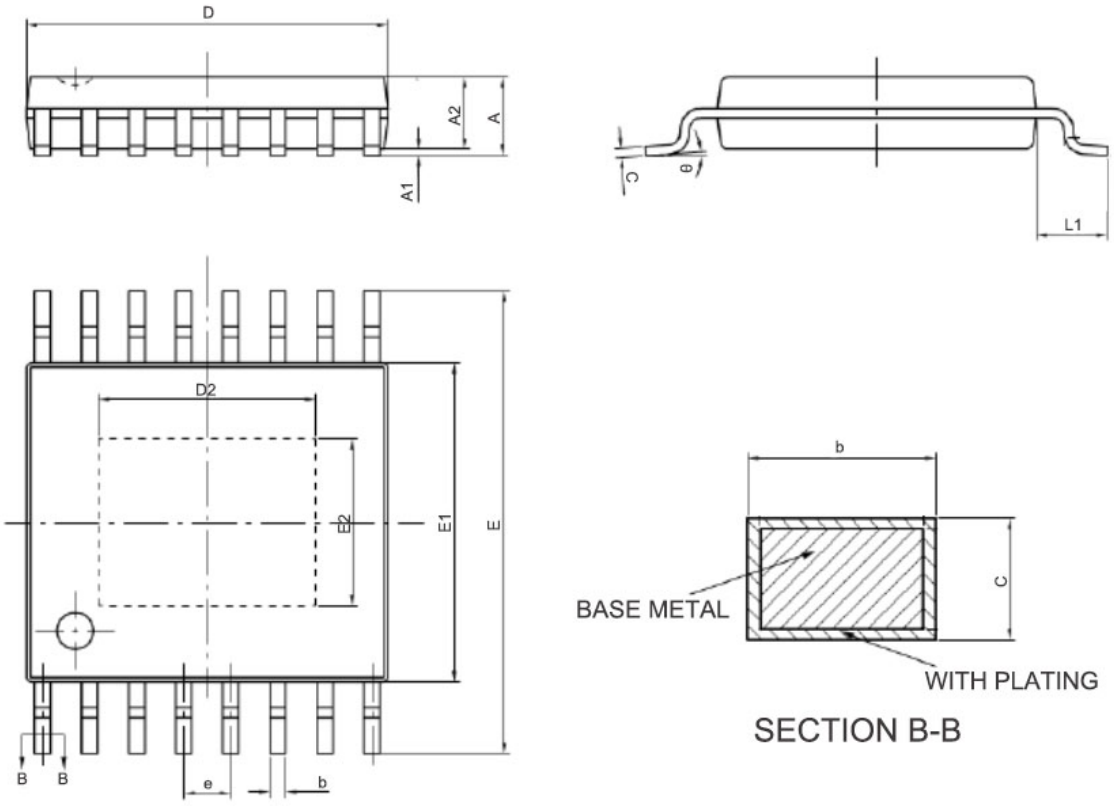
## *16 Pins, QFN (3x3) and (4x4)*




| Symbol | QFN (3x3) Dimensions | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | 0.02 | 0.05 |
| C | 0.18 | 0.20 | 0.25 |
| b | 0.18 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| D2 | 1.40 | 1.50 | 1.60 |
| E2 | 1.40 | 1.50 | 1.60 |
| e | 0.50 BSC. | | |
| L | 0.35 | 0.40 | 0.45 |
| **Symbol** | **QFN (4x4) Dimensions** | | |
| | **Min.** | **Nom.** | **Max.** |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | 0.02 | 0.05 |
| C | 0.18 | 0.20 | 0.25 |
| b | 0.25 | 0.30 | 0.35 |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| D2 | 2.10 | 2.20 | 2.30 |
| E2 | 2.10 | 2.20 | 2.30 |
| e | 0.65 BSC. | | |
| L | 0.35 | 0.40 | 0.45 |

Notes:
1. Refer to JEDEC MO-220 WEED-4 & WGGD-4
2. Unit: mm

## *16 Pins, TSSOP*




| Symbol | Dimensions | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.90 | 1.00 | 1.05 |
| b | 0.20 | - | 0.30 |
| e | 0.65 BSC | | |
| c | 0.13 | - | 0.19 |
| D | 4.86 | 4.96 | 5.06 |
| D2 | 2.90 | 3.00 | 3.10 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | 2.20 | 2.30 | 2.40 |
| L1 | 1.00 REF | | |
| θ | 0 | - | 8 |

Notes:
1. Refer to JEDEC MO-153
2. Unit: mm