

## 100V, 3A, Synchronous Buck Control

### 1 Features

- 12V to 100V wide operating input range
- 3A continuous output current capability
- Integrated 120V, 70mΩ high side and 120V, 70mΩ low side power MOSFET switches
- Adjustable Frequency from 50kHz to 500kHz Operation
- Precision Reference Voltage (1.2 V)
- Programmable Soft-Start with Pre-biased Load Capability
- Programmable EN Off Delay Function
- Programmable Over-Load Protection with 0.2S blank timer and Hiccup
- Programmable Cycle-by-Cycle Current Limiting Protection
- Programmable Input Under-Voltage Lockout Protection with Latch
- Programmable Input Over-Voltage Protection with Latch
- Output Over-Voltage Protection
- Over-Temperature Protection
- QFN5\*5mm-32

### 3 Description

PL89032 is a high voltage Buck Control designed for highperformance synchronous Buck DC/DC applications with inputvoltages up to 100V.

PL89032 integrates a high efficiency synchronous step-down switching regulator, which includes a 120V, 70mΩ high side and a 120V, 70mΩ low side MOSFETs to provide 3A continuous load current over12V to 100V wide operating input voltage.

PL89032 switching frequency is programmable from50 kHz up to 500 kHz allowing the flexibility to tune for efficiencyand size. The output voltage can be preciselyregulated using the internally 1.2 V reference voltage forlow voltage applications.

Protection features include userprogrammable undervoltage lockout, over voltage lockoutand over current protection.The supply current drops below 10μA in shutdown mode. PL89032 is a good choice for car infotainment application, telecom bus converter, etc.

### 2 Applications

- 48 V Non-Isolated DC-DC Converter
- Car applications
- Telecom Bus Converters
- General purpose
- USB Type-C Power Delivery
- Industrial DC-DC Motor Drivers

### 4 Typical Application Schematic

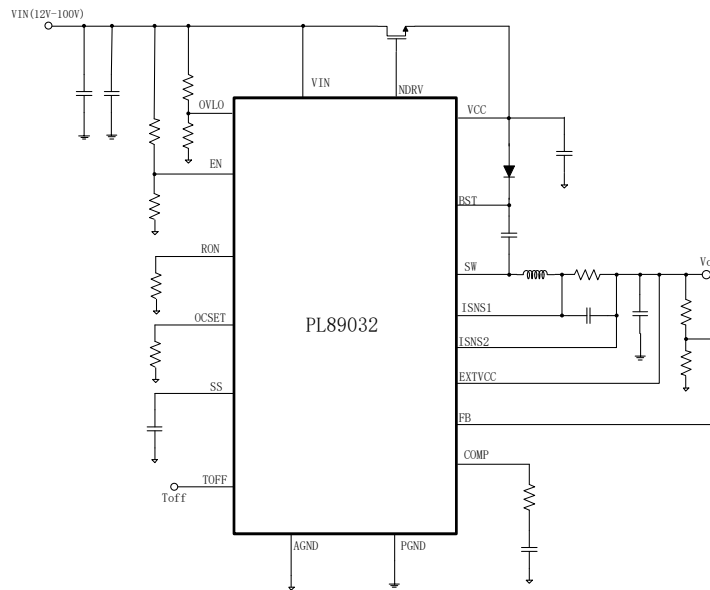


Fig. 1 Application Schemati

## 5 Pin Configuration and Functions

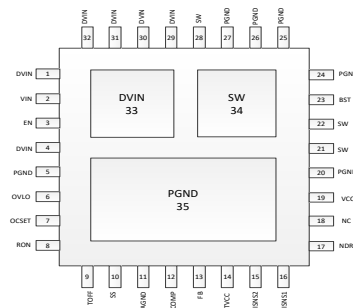


Fig. 2 QFN5\*5-32L Package (Top View)

| Pin    |                        | Description  |
|--------|------------------------|--|
| Name   | Number                 |  |
| VIN    | 2                      | Analog Input voltage.  |
| EN     | 3                      | Enable pin.  |
| DVIN   | 1,4,29,30,<br>31,32,33 | Power Input voltage.   |
| PGND   | 5,20,24,25,26,27,35    | Power Ground. This pin serves as a separate ground for the MOSFET driver and should be connected to the system's power ground plane.   |
| OVLO   | 6                      | An external voltage divider is used to set the over voltage threshold levels.  |
| OCSET  | 7                      | Current limit set point. A resistor from this pin to GND will set the positive and negative current limit threshold.   |
| RON    | 8                      | Connect this pin to GND by a resistor to set the switching frequency.  |
| TOFF   | 9                      | This pin provides user programmable shutdown delay time function.<br>Connect to GND: No Delay<br>Connect to VCC: 20S<br>Floating: 10S  |
| SS     | 10                     | This pin provides user programmable soft-start function. External capacitor connected from this pin to ground sets the startup time of the output voltage.   |
| AGND   | 11                     | Signal ground for internal reference and control circuitry.  |
| COMP   | 12                     | Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.   |
| FB     | 13                     | Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from noisy signal, such as SW and BST pin.  |
| EXTVCC | 14                     | External Power Input to an Internal LDO linear regulator. Connected to VCC. This LDO supplies VCC power from EXTVCC, bypassing the external NDRV LDO whenever EXTVCC is higher than 10V. Do not exceed 30V on this pin. Do not connect EXTVCC to a voltage greater than VIN. Connect to GND if not used. |
| ISNS2  | 15                     | Inductor current sense input 2.  |
| ISNS1  | 16                     | Inductor current sense input 1.  |
| NDRV   | 17                     | Drive Output for External Pass Device of the NDRV LDO Linear Regulator for VCC. Connect this pin to the gate of an external NMOS or NPN pass device.   |
| VCC    | 19                     | This pin provides power for the internal blocks of the IC. A minimum of 4.7uF capacitor must be connected from this pin to ground.   |
| SW     | 21,22,28,34            | Switch Node. Connect this pin to the switching node of inductor.   |
| BST    | 23                     | This pin powers the high side driver and must be connected to a voltage higher than input voltage. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to switch node.  |
| NC     | 18                     | Not Connected.   |

## 6 Device Marking Information

## PL89032

---

|         | Order Information | Package     | Package Qty | Top Marking     |
|---------|-------------------|-------------|-------------|-----------------|
| PL89032 | PL89032IQN32      | QFN5x5 - 32 | 5000        | 89032<br>RAAYMD |

**PL89032:** Part Number

**RAABB:** Lot Number. R: Year; AABB: Manufacturing Code

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(Note1)</sup>

|                 | PARAMETER  | MIN  | MAX                   | Unit |
|-----------------|--|------|-----------------------|------|
| Input Voltages  | V <sub>IN</sub> to GND   | -0.3 | 100                   | V    |
|                 | V <sub>FB</sub> , V <sub>OVLO</sub> , V <sub>UVLO</sub> to GND                     | -0.3 | 6                     |      |
|                 | V <sub>TOFF</sub> to GND   | -0.3 | 12                    |      |
|                 | V <sub>ISNS1,2</sub> to GND  | -0.3 | 65                    |      |
|                 | V <sub>EN</sub> to GND   | -0.3 | 100                   |      |
|                 | V <sub>EXTVCC</sub> to GND   | -0.3 | 30                    |      |
| Output Voltages | V <sub>VCC</sub> to GND  | -0.3 | 12                    | V    |
|                 | V <sub>RON</sub> , V <sub>OCSET</sub> , V <sub>SS</sub> , V <sub>COMP</sub> to GND | -0.3 | 6                     |      |
|                 | V <sub>BST</sub> to V <sub>SW</sub>  | -0.3 | 12                    |      |
|                 | V <sub>SW</sub> to GND   | -3   | V <sub>IN</sub> + 0.3 |      |

### 7.2 Handling Ratings

| PARAMETER        | DEFINITION                | MIN | MAX  | UNIT |
|------------------|---------------------------|-----|------|------|
| T <sub>ST</sub>  | Storage Temperature Range | -65 | 150  | °C   |
| T <sub>J</sub>   | Junction Temperature      |     | +150 | °C   |
| T <sub>L</sub>   | Lead Temperature          |     | +260 | °C   |
| V <sub>ESD</sub> | HBM Human body model      |     | 2    | kV   |
|                  | CDM Charger device model  |     | 500  | V    |

### 7.3 Recommended Operating Conditions<sup>(Note 2)</sup>

|                 | PARAMETER  | MIN  | MAX                  | Unit |
|-----------------|--|------|----------------------|------|
| Input Voltages  | V <sub>IN</sub> to GND   | 12   | 100                  | V    |
|                 | V <sub>FB</sub> , V <sub>OVLO</sub> , V <sub>UVLO</sub> to GND                     | -0.3 | 5                    |      |
|                 | V <sub>TOFF</sub> to GND   | -0.3 | 10                   |      |
|                 | V <sub>ISNS1,2</sub> to GND  | -0.3 | 60                   |      |
|                 | V <sub>EN</sub> to GND   | -0.3 | 100                  |      |
|                 | V <sub>EXTVCC</sub> to GND   | -0.3 | 30                   |      |
| Output Voltages | V <sub>VCC</sub> to GND  | -0.3 | 10                   | V    |
|                 | V <sub>RON</sub> , V <sub>OCSET</sub> , V <sub>SS</sub> , V <sub>COMP</sub> to GND | -0.3 | 5                    |      |
|                 | V <sub>BST</sub> to V <sub>SW</sub>  | -0.3 | 10                   |      |
|                 | V <sub>SW</sub> to GND   | -3   | V <sub>IN</sub> +0.3 |      |
| Temperature     | Operating junction temperature range, T <sub>J</sub>                               | -40  | +125                 | °C   |

### 7.4 Thermal Information(Note 4)

| Symbol          | Description                            | QFN5x5 - 32 | Unit |
|-----------------|--|-------------|------|
| θ <sub>JA</sub> | Junction to ambient thermal resistance | 40          | °C/W |
| θ <sub>JC</sub> | Junction to case thermal resistance    | 23          |      |

#### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The device function is not guaranteed outside of the recommended operating conditions.
- 3) Measured on approximately 1" square of 1 oz copper.

| SYMBOL                                 | PARAMETER   | CONDITION  | MIN   | TYP | MAX   | UNIT |
|--|---|--|-------|-----|-------|------|
| V <sub>IN</sub>                        | Input Supply Operating Voltage Range  |  | 12    |     | 100   | V    |
| V <sub>OUT</sub>                       | Regulated Output Voltage Set Point  |  | 1.2   |     | 60    | V    |
| <b>MOSFET</b>                          |   |  |       |     |       |      |
| R <sub>DS(ON)_H</sub>                  | High-Side Switch On-Resistance  | I <sub>OUT</sub> = 1A, V <sub>OUT</sub> = 5V   |       | 70  |       | mΩ   |
| R <sub>DS(ON)_L</sub>                  | Low-Side Switch On-Resistance   | I <sub>OUT</sub> = 1A, V <sub>OUT</sub> = 5V   |       | 70  |       | mΩ   |
| <b>REFERENCE VOLTAGE</b>               |   |  |       |     |       |      |
| I <sub>Q</sub>                         | Statics Current   | Open Loop, V <sub>FB</sub> = 1.25V, No Switching, V <sub>IN</sub> =48V, T <sub>J</sub> =25°C |       | 400 |       | uA   |
| I <sub>SHUTDOWN</sub>                  | EN Shutdown Supply Current  | Close Loop, V <sub>EN</sub> =0V, V <sub>IN</sub> =48V  |       | 20  |       |      |
| <b>REFERENCE VOLTAGE</b>               |   |  |       |     |       |      |
| V <sub>FB</sub>                        | Feedback Voltage  |  |       | 1.2 |       | V    |
|  | Accuracy  |  | -1.5  |     | +1.5  | %    |
| <b>SUPPLY VOLTAGE (V<sub>CC</sub>)</b> |   |  |       |     |       |      |
| V <sub>CC</sub>                        | V <sub>CC</sub> Regulator Output  | Supply by NDRV LDO   | 9     | 9.5 | 10    | V    |
|  |   | Supply by EXTVCC LDO   | 9.5   | 10  | 10.5  | V    |
| <b>UNDERVOLTAGE LOCKOUT</b>            |   |  |       |     |       |      |
| V <sub>VCC_UVLO</sub>                  | V <sub>CC</sub> Under Voltage Lockout Voltage(V <sub>CC</sub> increasing)             | -40°C ≤ T <sub>J</sub> ≤ 125°C   |       | 8   |       | V    |
| V <sub>VCC_UVLOH</sub>                 | V <sub>CC</sub> Under Voltage Hysteresis  |  |       | 670 |       | mV   |
| V <sub>BST_UVLO</sub>                  | V <sub>BST</sub> Under Voltage Lockout Voltage(V <sub>BST</sub> increasing)           | -40°C ≤ T <sub>J</sub> ≤ 125°C   |       | 5.6 |       | V    |
| V <sub>BST_UVLOH</sub>                 | V <sub>BST</sub> Under Voltage Hysteresis   |  |       | 860 |       | mV   |
| V <sub>IN_UVLO</sub>                   | V <sub>IN</sub> Under Voltage Lockout Voltage(V <sub>IN</sub> increasing)             |  |       | 6.5 |       | V    |
| V <sub>IN_UVLOH</sub>                  | V <sub>IN</sub> Under Voltage Hysteresis  |  |       | 650 |       | mV   |
| V <sub>EN_UVLO</sub>                   | EN Under Voltage Lockout Voltage(V <sub>EN</sub> increasing)                          |  |       | 1.2 |       | V    |
| V <sub>EN_UVLOH</sub>                  | EN Under Voltage Hysteresis   |  |       | 200 |       | mV   |
| <b>OVER VOLTAGE LOCKOUT</b>            |   |  |       |     |       |      |
| REF <sub>IN_OVP</sub>                  | Reference of V <sub>IN</sub> Over Voltage Lockout Voltage(V <sub>IN</sub> increasing) |  | 1.176 | 1.2 | 1.224 | V    |
| HYS <sub>IN_OVP</sub>                  | Reference Hysteresis of V <sub>IN</sub> Over Voltage Lockout Voltage                  |  |       | 200 |       | mV   |
| <b>CONTROL LOOP</b>                    |   |  |       |     |       |      |
| I(Source/Sink)                         | Source/Sink Current   |  |       | 300 |       | uA   |
| gm                                     | Trans-conductance   |  |       | 3   |       | mS   |
| <b>SOFT-START</b>                      |   |  |       |     |       |      |
| I <sub>SS</sub>                        | Soft-Start Current  | SS = 0 V   | 15    | 20  | 25    | uA   |
| <b>VSNS LIMIT</b>                      |   |  |       |     |       |      |
| V <sub>OCSET</sub>                     | OCSET voltage   | -40°C ≤ T <sub>J</sub> ≤ 125°C   |       | 1.2 |       | V    |
| V <sub>LIMH</sub>                      | On Duty ISNS1-ISNS2 Limit   | R <sub>OCSET</sub> = 25k Ohm, V <sub>LIMH</sub> =1.2/R <sub>OCSET</sub> *25K/10              |       | 120 |       | mV   |
| V <sub>LIML</sub>                      | Off Duty ISNS1-ISNS2 Limit  | R <sub>OCSET</sub> = 25k Ohm, V <sub>LIML</sub> =1.2/R <sub>OCSET</sub> *20K/10              |       | 96  |       | mV   |
| T <sub>OVERLOAD</sub>                  | Over Load Protection Blank Time   |  |       | 200 |       | ms   |
| <b>Frequency</b>                       |   |  |       |     |       |      |

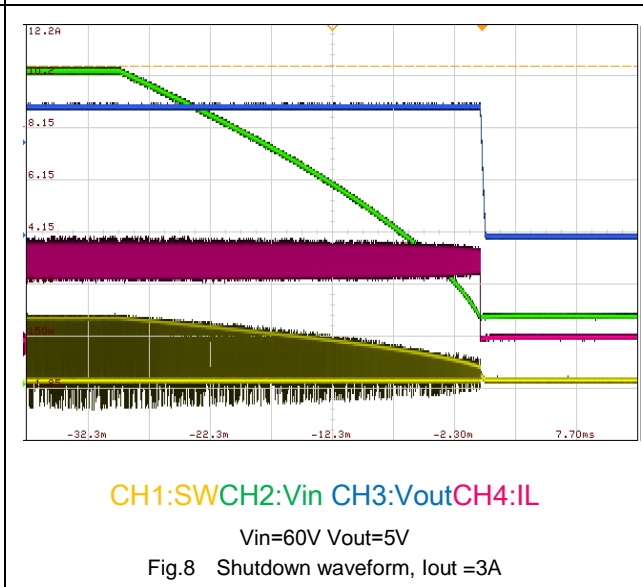
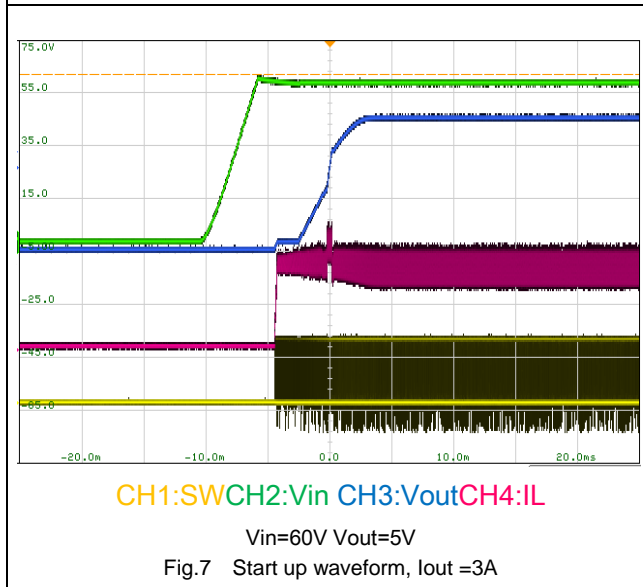
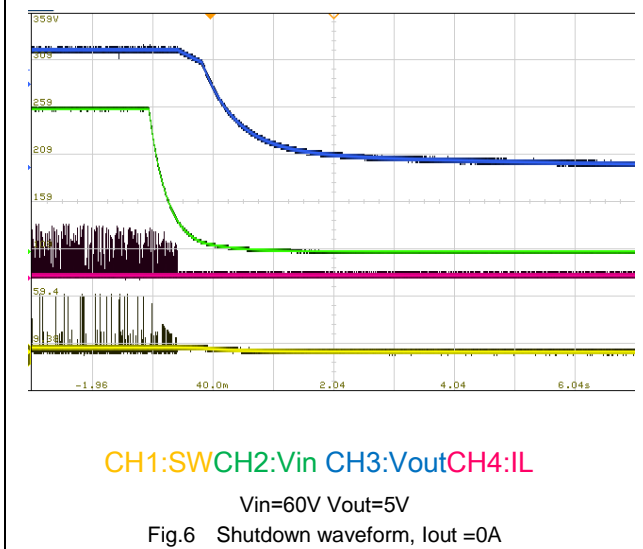
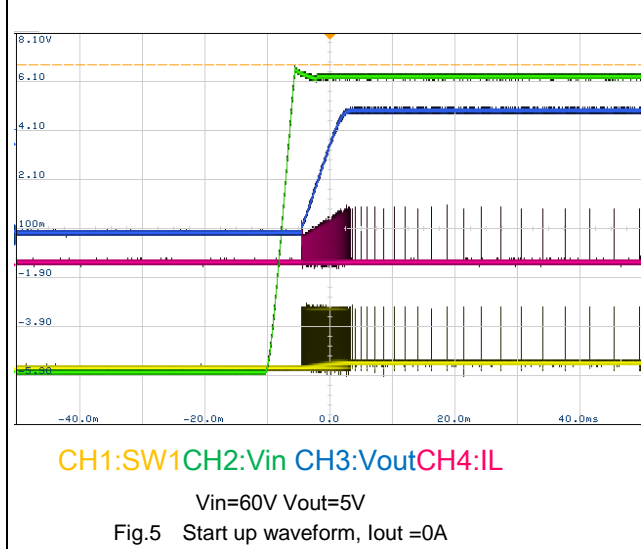
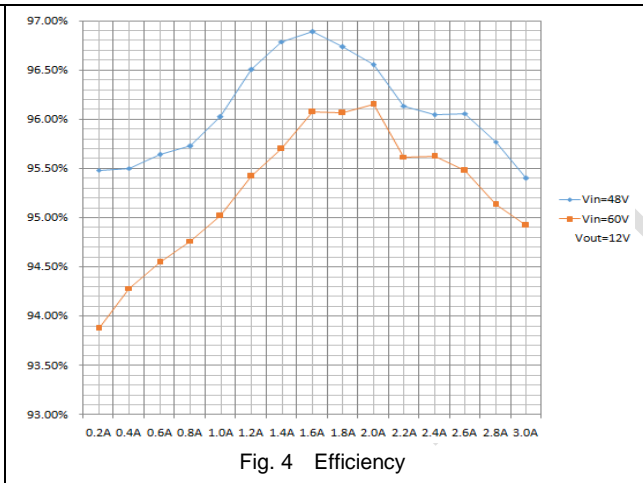
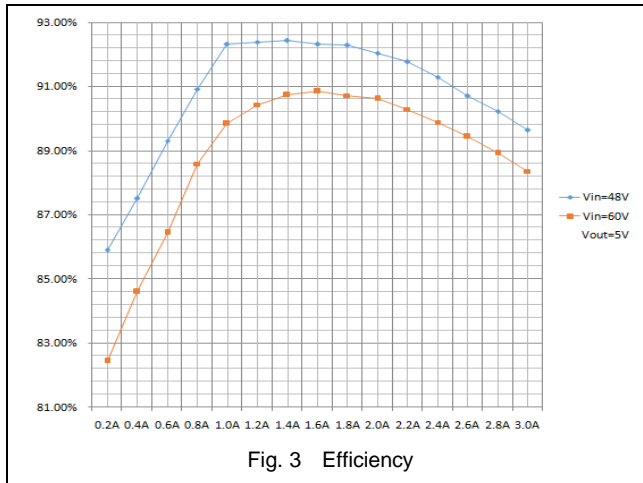
## PL89032

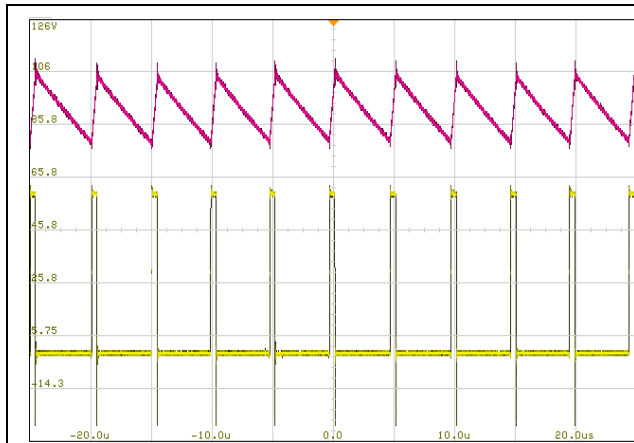
|                       |                                      |  |                  |     |
|-----------------------|--------------------------------------|--|------------------|-----|
| F <sub>SW</sub>       | Switching Frequency                  | $F_{sw} = V_{out} / (R_h * 500p)$<br>Or $F_{sw} = 1 / (R_L * 50p)$ | 50    200    500 | kHz |
| TON <sub>MIN</sub>    | Minimum On Time                      |  | 140              | ns  |
| TOFF <sub>MIN</sub>   | Minimum Off Time                     |  | 400              | ns  |
| <b>Toff Timer</b>     |                                      |  |                  |     |
| T <sub>OFF</sub>      | Toff Time Delay                      | Toff = GND   | 0                | s   |
|                       |                                      | Toff = Float   | 10               | s   |
|                       |                                      | Toff = VCC   | 20               | s   |
| <b>OUTPUT DRIVERS</b> |                                      |  |                  |     |
| Tdelay1               | Top Gate Off to Bottom Gate On Delay |  | 70               | ns  |
| Tdelay2               | Bottom Gate Off to Top Gate On Delay |  | 70               | ns  |

**Note:**

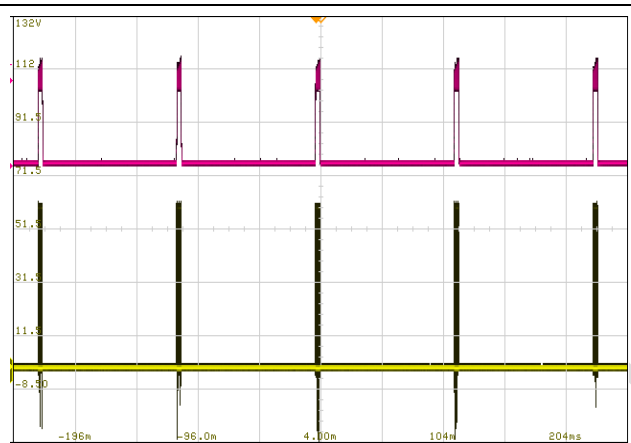
4) Guaranteed by design, not tested in production.

## 8 Typical Characteristics

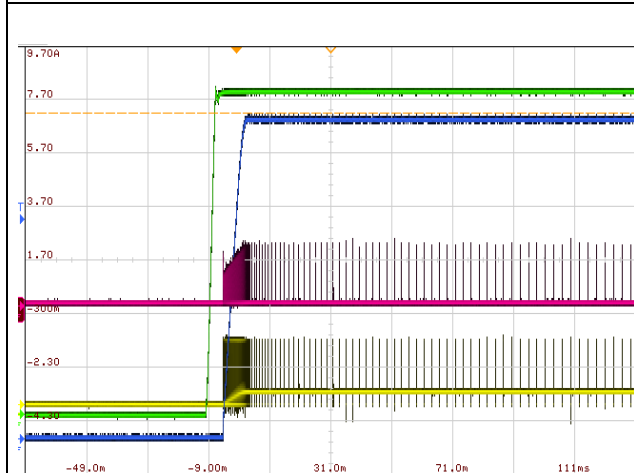




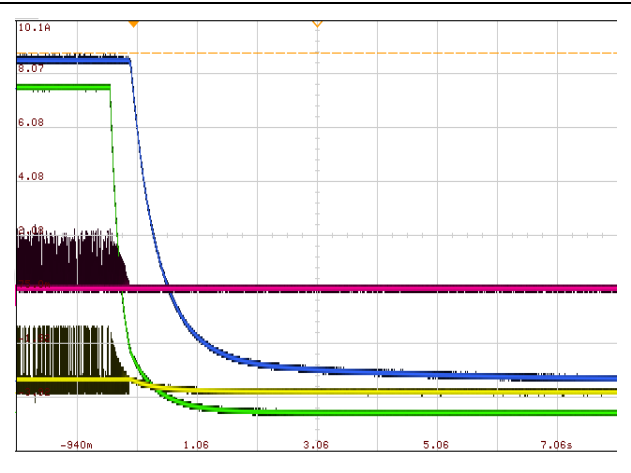
CH1:SWCH4:IL  
Vin=60V Vout=5V  
Fig.9 SW waveform, Iout =3A



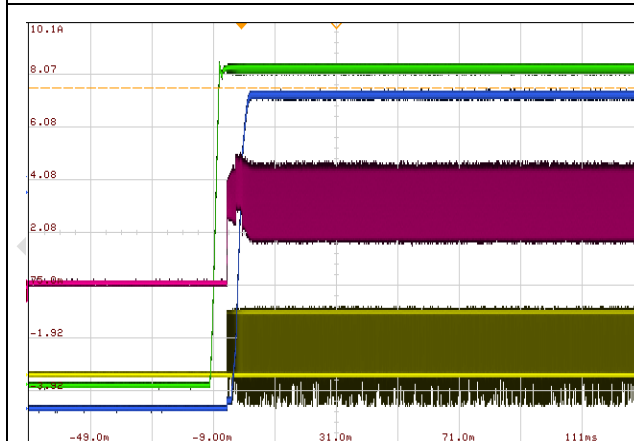
CH1:SWCH4:IL  
Vin=60V Vout=5V  
Fig.10 Short Circuit waveform, Iout =3A



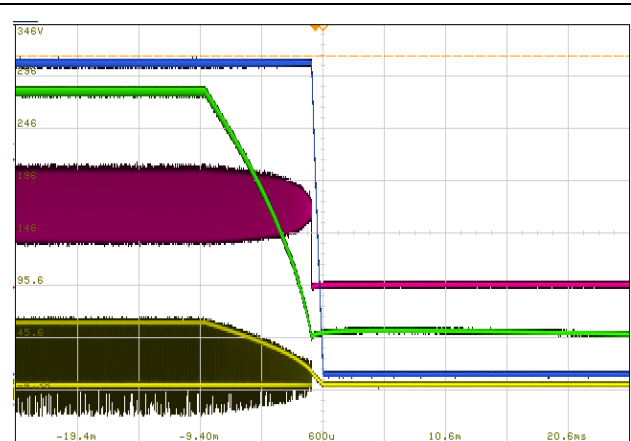
CH1:SWCH2:Vin CH3:VoutCH4:IL  
Vin=60V Vout=12V  
Fig.11 Start up waveform, Iout =0A



CH1:SWCH2:Vin CH3:VoutCH4:IL  
Vin=60V Vout=12V  
Fig.12 Shut down waveform, Iout =0A



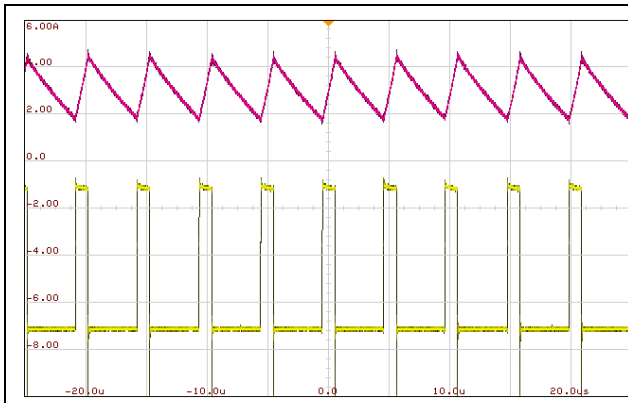
CH1:SWCH2:Vin CH3:VoutCH4:IL  
Vin=60V Vout=12V  
Fig.13 Start up waveform, Iout =3A



CH1:SWCH2:Vin CH3:VoutCH4:IL  
Vin=60V Vout=12V  
Fig.14 Shut down waveform, Iout =3A

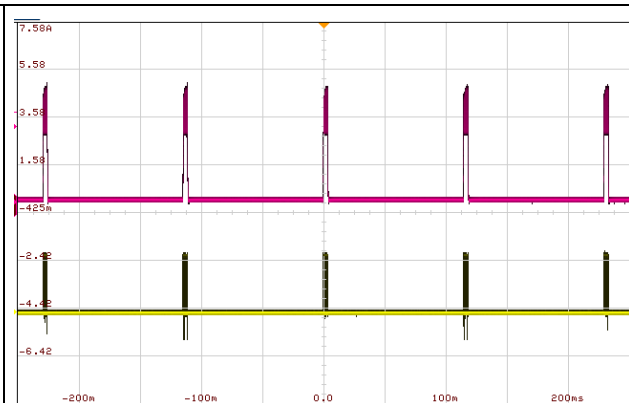


# PL89032



CH1:SWCH4:IL

Vin=60V Vout=12V  
Fig.15SW waveform, Iout =3A



CH1:SWCH4:IL

Vin=60V Vout=12V  
Fig.16 Short Circuit waveform, Iout =3A

# PL89032

## 9 Detailed Description

### 9.1 Overview

PL89032 is a high voltage Buck Control designed for highperformance synchronous Buck DC/DC applications with inputvoltages up to 100V.

PL89032 integrates a high efficiency synchronous step-down switching regulator, which includes a 120V, 70mΩ high side and a 120V, 70mΩ low side MOSFETs to provide 3A continuous load current over 12V to 100V wide operating input voltage.

The PL89032 adopts adaptive constant on time peak current mode control at the moderate to heavy load currents and operates inthe PFM mode at the light load current. With this control scheme, the PL89032 provides the excellent line and load transientresponse with the minimal output capacitor. The external loop compensation brings the flexibility to use awider range of the inductor and output capacitor combinations.

The PL89032 supports the adjustable switching frequency up to 500kHz. This device implements user programmable cycle-by-cycle current limit with 200ms over load timer to protect the device from thermal run away. If the overload condition or short circuit protection is triggered, enter hiccup mode until the fault is removed. This device also implements user programmable over voltage lockout protection and over temperature protection to ensure reliably operation.

### 9.2 Functional Block Diagram

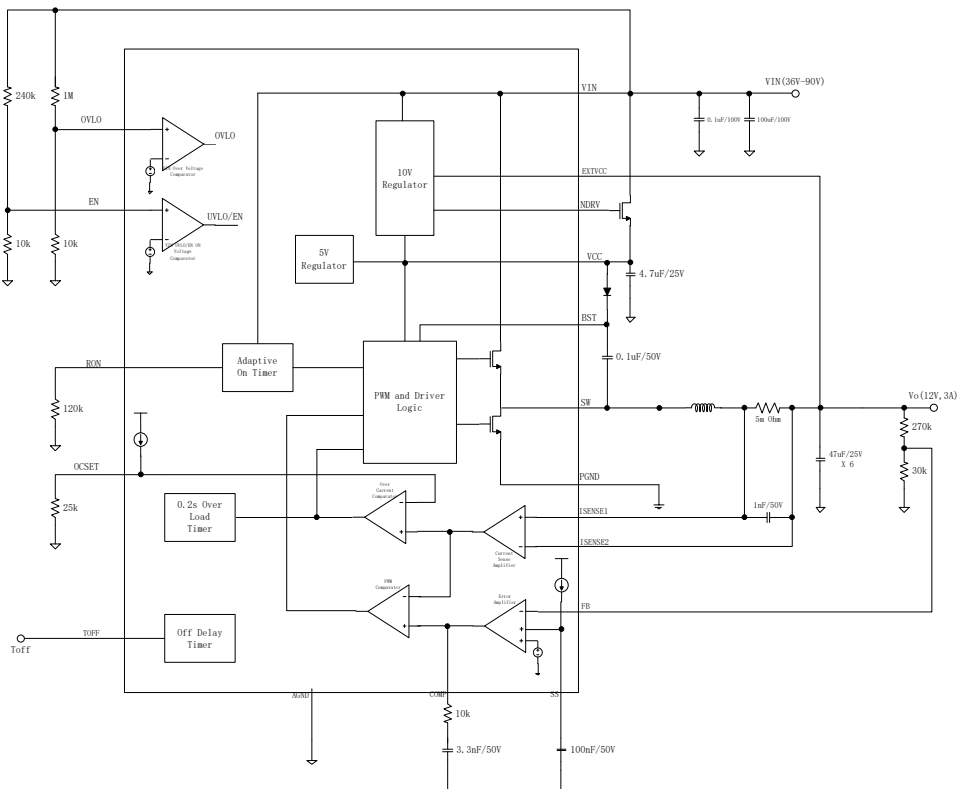


Fig. 21 Functional Block Diagram

## 9.3 Feature Description

### 9.3.1 Enable and OVLO

When the EN pin is pulled high above 1.2V, this part is enabled. When the EN pin is pulled below 1.0V, this part goes into the shutdown mode and stops operation.

When the OVLO pin is pulled high above 1.2V, the PL89032 is disabled and it will not resume switching even if OVLO falls below 1.0V unless EN is toggled.

### 9.3.2 Under-voltage Lockout

This controller stops switching when the input voltage drops below 5.85V or VCC is below 7.33V. It resumes operation when input voltage is larger than 6.5V and VCC is larger than 8V.

### 9.3.3 Cycle-by-Cycle Current Limit and Over Load Protection

The PL89032 provides cycle-by-cycle current limit to protect power MOSFET during on duty and also off duty. It will immediately turn off high side MOSFET once on duty current limit is triggered or prolongs the off duty until the inductor current is lower than off duty current limit. Hiccup protection will be triggered if the over current condition endures more than 200mS. And the switching will be resumed after 16 soft start procedures.

### 9.3.4 Programmable Switching Frequency

This controller features a programmable switching frequency ranging from 50kHz to 500kHz.

The frequency setting by RON is calculated as below:

$$F_{SW} = \frac{V_{OUT}}{R_{ON} (k\Omega) \times 0.5} (\text{MHz}) (1)$$

### 9.3.5 Error Amplifier

The PL89032 has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is 3 mA / V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

### 9.3.6 VCC Regulators

The PL89032 contains two VCC regulators that provide power supply for low side gate driver and boot-strap high side gate drive. One is the NDRV regulator which regulates VCC to 9.5V. The other one is the 10V low dropout LDO powered by EXT VCC which is current limited to 60mA. The VCC load current should be evaluated if NDRV regulator is not used.

### 9.3.7 Bootstrap Voltage (BST)

The PL89032 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100 nF. A ceramic capacitor with an X7R or X5R

## PL89032

---

grade dielectric with a voltage rating of 25 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

### 9.3.8 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 130°C.

## 10 Application and Implementation

### 10.1 Setting the switching Frequency

The switching frequency of the PL89032 can be programmed as equation 1. For a target switching frequency of 200 kHz, The calculated value is 120 kΩ.

### 10.2 Setting the Output Current Limit

The cycle-by-cycle current limit of the PL89032 is configured by combination of Rocset between OCSET and AGND and sense resistor Rsns in serial with inductor. The cycle-by-cycle current limit is determined as follows:

$$I_{LIMIT} = \frac{2.4}{R_{OCSET} (k\Omega) \times R_{SNS} (\Omega)} (A) (2)$$

### 10.3 Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. A value between 10k and 1M is recommended for both resistors. If R1=200k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) (3)$$

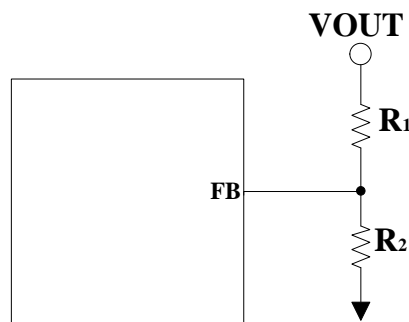


Fig. 22

### 10.4 Selecting the Inductor

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{0.4 \times F_{SW} \times I_{OUT\_MAX}} (4)$$

where  $F_{SW}$  is the switching frequency and  $I_{OUT\_MAX}$  is the maximum load current.

PL89032 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.
- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 10\text{m}\Omega$  to achieve a good overall efficiency.

### **10.5 Selecting the Output Capacitors**

The Output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor.

### **10.6 Selecting the Input Capacitors**

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-down converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a  $10\text{-}\mu\text{F}$  input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

### **10.7 Selecting the Bootstrap Capacitor**

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is  $0.1\mu\text{F}$  to  $1\mu\text{F}$ . CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of  $0.1\mu\text{F}$  was selected for this design example.

### **10.8 Selecting the VCC Capacitors**

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of CVCC should be at least 10 times greater than the value of CBST, and should be a good quality, low ESR, ceramic capacitor. CVCC should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of  $4.7\mu\text{F}$  was selected for this design example.

## 10.9 Design Example

The Figure 5 is the typical application schematic for 36 to 90-V input to output 12-V output converter.

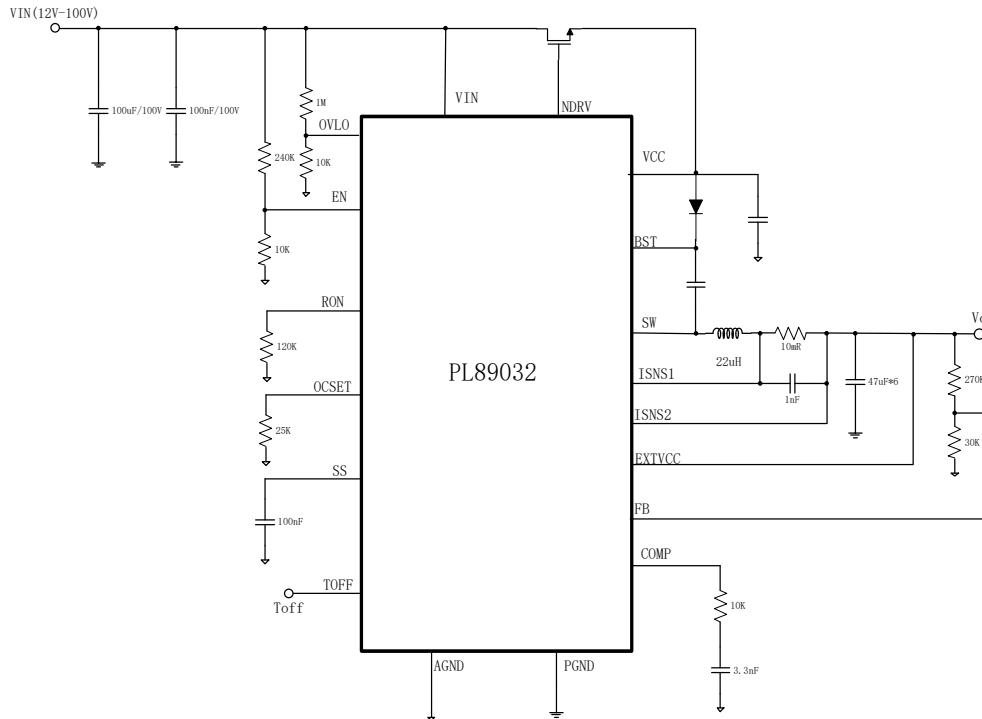


Figure 23. Application Schematic

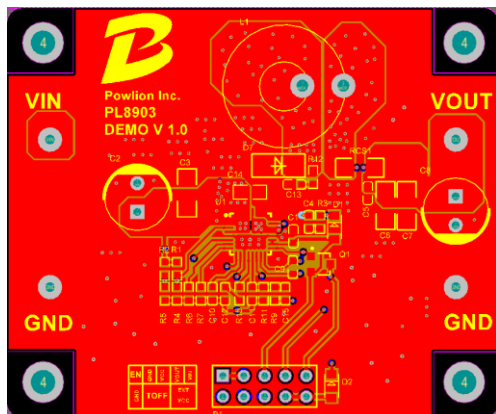


Fig. 24 Toplayer

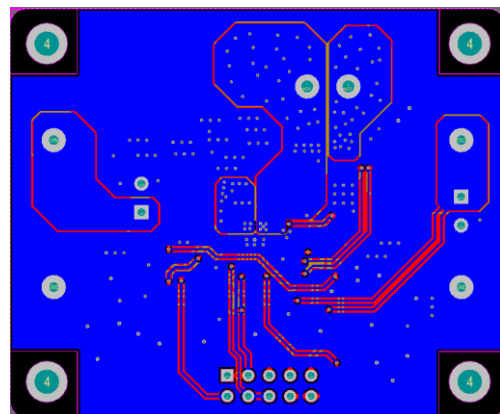
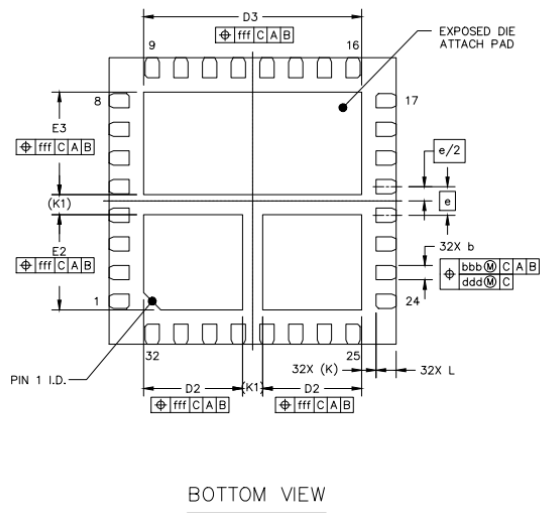
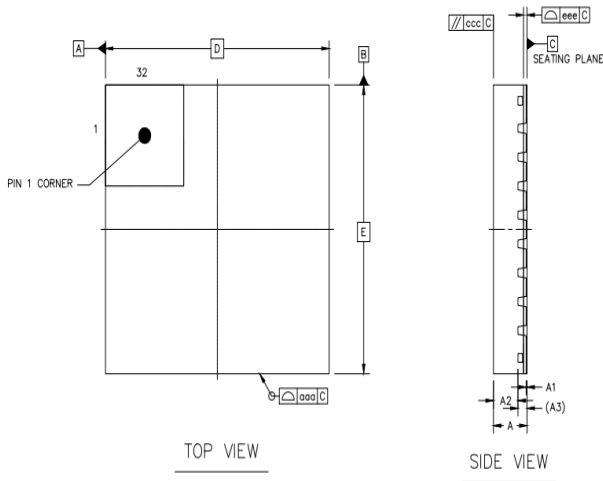


Fig. 25 Bottomlayer

**11 Packaging Informatio**



|                              |   | SYMBOL | MIN       | NOM   | MAX   |
|------------------------------|---|--------|-----------|-------|-------|
| TOTAL THICKNESS              |   | A      | 0.7       | 0.75  | 0.8   |
| STAND OFF                    |   | A1     | 0         | 0.02  | 0.05  |
| MOLD THICKNESS               |   | A2     | ---       | 0.55  | ---   |
| L/F THICKNESS                |   | A3     | 0.203 REF |       |       |
| LEAD WIDTH                   |   | b      | 0.2       | 0.25  | 0.3   |
| BODY SIZE                    | X | D      | 5 BSC     |       |       |
|                              | Y | E      | 5 BSC     |       |       |
| LEAD PITCH                   |   | e      | 0.5 BSC   |       |       |
| EP SIZE                      | X | D2     | 1.625     | 1.725 | 1.825 |
|                              | Y | E2     | 1.56      | 1.66  | 1.76  |
|                              | X | D3     | 3.7       | 3.8   | 3.9   |
|                              | Y | E3     | 1.69      | 1.79  | 1.89  |
| LEAD LENGTH                  |   | L      | 0.25      | 0.35  | 0.45  |
| LEAD TIP TO EXPOSED PAD EDGE |   | K      | 0.25 REF  |       |       |
|                              |   | K1     | 0.35 REF  |       |       |
| PACKAGE EDGE TOLERANCE       |   | aaa    | 0.1       |       |       |
| MOLD FLATNESS                |   | ccc    | 0.1       |       |       |
| COPLANARITY                  |   | eee    | 0.08      |       |       |
| LEAD OFFSET                  |   | bbb    | 0.1       |       |       |
|                              |   | ddd    | 0.05      |       |       |
| EXPOSED PAD OFFSET           |   | fff    | 0.1       |       |       |
|                              |   |        |           |       |       |
|                              |   |        |           |       |       |
|                              |   |        |           |       |       |
|                              |   |        |           |       |       |

**IMPORTANT NOTICE**

Powlicon Inc. assumes no responsibility for any errors which may appear in this document. Powlicon Inc. reserves the right to change devices or specifications detailed herein at any time without notice. Powlicon Inc. does not assume any liability arising out of the application or use of any product described herein; neither it does it convey any license under its patent rights, nor the rights of others. Powlicon Inc. products are not authorized for use as critical components in life support devices or systems without written approval letter from the Chief Executive Officer of Powlicon Inc.. The use of products in such applications shall assume all risks of such use and will agree to not hold against Powlicon Inc. for all damages.